Department of Electrical and Electronics Engineering

Curriculum for M.E. Applied Electronics

Regulations 2014 - Revision 0

Semester I

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
140AE0101	Applied Mathematics	3	1	0	4	100
140AE0102	Advanced Digital Signal Processing	3	1	0	4	100
140AE0103	Advanced Digital System Design	3	0	0	3	100
140AE0104	VLSI Design Techniques	3	0	0	3	100
140AE0105	Industrial Electronics	3	0	0	3	100
xxx	Elective– I	3	0	0	3	100
PRACTICAL						
140AE0107	Applied Electronics Design Laboratory I	0	0	3	2	100
Total		**18**	**2**	**3**	**22**	**700**

SEMESTER II

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
140AE0201	Analysis and Design of Analog Integrated Circuits	3	1	0	4	100
140AE0202	Embedded Systems	3	0	0	3	100
140AE0203	CAD of VLSI Circuits	3	0	0	3	100
140AE0204	Digital Control Engineering	3	0	0	3	100
xxx	Elective– II	3	0	0	3	100
xxx	Elective –III	3	0	0	3	100
PRACTICAL						
140AE0207	Applied Electronics Design Laboratory II	0	0	3	2	100
Total		**18**	**1**	**3**	**21**	**700**

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SEMESTER III

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
xxx	Elective –IV	3	0	0	3	100
xxx	Elective –V	3	0	0	3	100
xxx	Elective– VI	3	0	0	3	100
PRACTICAL						
140AE0307	Project Work Phase I	0	0	12	6	200
TOTAL		**9**	**0**	**12**	**15**	**500**

SEMESTER IV

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
PRACTICAL						
140AE0407	Project Work Phase II	0	0	24	12	400
TOTAL		**0**	**0**	**24**	**12**	**400**

Total Credits: 70

LIST OF ELECTIVES

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
140AE9111	Project Management	3	0	0	3	100
140AE9112	Advanced Microprocessors	3	0	0	3	100
140AE9113	Programming with VHDL	3	0	0	3	100
140AE9114	Digital Image Processing	3	0	0	3	100
140AE9115	Soft Computing Techniques	3	0	0	3	100
140AE9116	Power Quality Engineering	3	0	0	3	100
140AE9117	ASIC Design	3	0	0	3	100
140AE9118	Data Communication Networks	3	0	0	3	100
140AE9119	Virtual Instrumentation Systems	3	0	0	3	100
140AE9120	Nano computing	3	0	0	3	100
140AE9121	VLSI Signal Processing	3	0	0	3	100
140AE9122	High Performance Switching Architectures	3	0	0	3	100
140AE9123	MEMS System Design Concepts	3	0	0	3	100
140AE9124	Wavelet Transforms and its Applications	3	0	0	3	100
140AE9125	Low Power VLSI Design	3	0	0	3	100
140AE9126	Internetworking and multimedia	3	0	0	3	100
140AE9127	Algorithm Analysis and Design	3	0	0	3	100
140AE9128	Research Methodology	3	0	0	3	100
140AE9129	Speech and Audio Signal Processing	3	0	0	3	100

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SEMESTER I

140AE0101 **APPLIED MATHEMATICS** **3 1 0 4**

AIM:

To enhance the mathematical knowledge of the students and develop the skills in determining the solutions of problems related to their field.

OBJECTIVES:

- To introduce the fundamental ideas of linear algebra.
- To introduce the concepts of eigen values and eigen vectors.
- To introduce the concepts of linear programming and non linear programming.

UNIT I LINEAR EQUATIONS AND VECTOR SPACES **9+3**

System of linear equations – Row reduction and Echelon forms – Application of linear systems –Vector spaces and subspaces and linear transformations – Linearly independent sets; Bases Dimension of a vector space – Coordinate systems.

UNIT II MATRIX ALGEBRA **9+3**

Inverse of a matrix – Characteristics of invertible matrices – Partitioned matrices – Matrix factorizations – Dimension and rank – Eigen values & Eigen vectors – Characteristic equation – Diagonalization of symmetric matrices – Quadratic forms – Applications to differential equations – Iterative estimates for Eigen values – Applications to image processing.

UNIT III ORTHOGONALITY AND LEAST SQUARES **9+3**

Inner product, length and Orthogonality – Orthogonal sets – Orthogonal projections – Gram – Schmidt process – Least square problems – Inner product spaces – Applications of inner product spaces.

UNIT IV LINEAR PROGRAMMING **9+3**

Simplex algorithm – Two–phase and Big–M method – Duality theory – Dual simplex method – Transportation and Assignment problems.

UNIT V NON – LINEAR PROGRAMMING **9+3**

Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Saddle point problem – Graphical method of non–linear programming problem involving only two variables – Kuhn–tucker conditions with non–negative constraints – Wolfe's modified simplex method.

L: 45, T: 15, Total: 60

REFERENCES:

1. David C Lay, "Linear Algebra and its Applications", Pearson Education Asia, New Delhi, 2003.
2. Gilbert Strang, "Linear Algebra and its Applications", Brooks/Cole Ltd., New Delhi, 3rd Edition, 2003.
3. Seymour Lipschutz and Marc Lipson, "Schaum's Outline of Linear Algebra", McGraw Hill Trade,New Delhi, 3rd Edition, 2000.
4. Howard A Anton "Elementary Linear Algebra", John Wiley & Sons, Singapore, 8th Edition 2000.
5. Gupta. P.K, Hira. D.S, "Operations Research", S.Chand &Co ., 1999.

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140AE0102 ADVANCED DIGITAL SIGNAL PROCESSING 3 1 0 4
(Common to AE and CM Programmes)

AIM:
To provide students with a solid understanding of a number of important and related advanced topics in digital signal processing such as filters, power spectrum estimation, signal modeling and adaptive filtering.

OBJECTIVES:
- Understand the concepts of discrete random processes.
- Compute the spectral estimation by non parametric methods.
- Apply various estimators and predictor to filters.
- Compare FIR and IIR adaptive filters.
- Know the concepts of multirate DSP.
- Application of sub–band coding.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9+3
Discrete Random Processes – Ensemble Averages, Stationary processes, Bias and Estimation, Auto covariance, Autocorrelation, Parseval's theorem, Wiener – Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION 9+3
Estimation of spectra from finite duration signals, Nonparametric methods – Periodogram, Modified periodogram, Bartlett, Welch and Blackman –Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson–Durbin algorithm.

UNIT III LINEAR ESTIMATION AND PREDICTION 9+3
Linear prediction – Forward and Backward prediction, Solution of Prony's normal equations, Least mean squared error criterion, Wiener filter for filtering and prediction, FIR and IIR Wiener filters, Discrete Kalman filter.

UNIT IV ADAPTIVE FILTERS 9+3
FIR adaptive filters – adaptive filter based on steepest descent method – Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive filters, Exponentially Weighted RLS, Sliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9+3
Mathematical description of change of sampling rate – Interpolation and Decimation, Decimation by an integer factor, Interpolation by an integer factor, sampling rate conversion by a rational factor, Polyphase filter structures, Multistage implementation of Multirate system, Application to subband coding – Wavelet transform.

L: 45, T: 15, Total: 60

REFERENCES:

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2007.
3. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education Inc., 2nd Edition, 2004 (For Wavelet Transform Topic).

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BoS Chairman

140AE0103 **ADVANCED DIGITAL SYSTEM DESIGN** **3 0 0 3**

AIM:

To enhance the knowledge to the students about advanced digital circuit design and its fault identification and the VHDL language for its design.

OBJECTIVES:

- To design and analyze the synchronous and asynchronous sequential circuits.
- To introduce the concepts of fault diagnosis and testability algorithms in digital circuit.
- To implement the logic circuit design in programmable devices.
- To give an exposure to the VHDL language.

UNIT I SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of clocked synchronous sequential circuits and modeling – State diagram, state table, state table assignment and reduction – Design of synchronous sequential circuits – design of iterative circuits – ASM chart and realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of asynchronous sequential circuit – flow table reduction – races – state assignment –transition table and problems in transition table – design of asynchronous sequential circuit – Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS **9**

Fault table method–path sensitization method – Boolean difference method – D algorithm –Tolerance techniques – The compact algorithm – Fault in PLA – Test generation – DFT schemes – Built in self test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES **9**

Programming Techniques – Re–Programmable Devices Architecture – Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT V NEW GENERATION PROGRAMMABLE LOGIC DEVICES **9**

Foldback Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 – Xilinx 3000.

L: 45, T: 0, Total: 45

REFERENCES:

1. Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Deisgn", Tata McGraw Hill, 2002.
3. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education, 2004.
4. Parag K Lala, "Digital System design using PLD", BS Publications, 2003.
5. John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001.
6. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001.
7. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

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BoS Chairman

140AE0104 **VLSI DESIGN TECHNIQUES** **3 0 0 3**

AIM:

To enhance the knowledge on VLSI design techniques and Verilog HDL to the students.

OBJECTIVES:

- To introduce the concepts of VLSI technology and circuit design processes.
- To introduce the concepts of VLSI fabrication technology.
- To provide an exposure to the students on design of various VLSI based systems.
- To give an exposure to the students on Verilog HDL.

UNIT I OVERVIEW OF VLSI DESIGN TECHNOLOGY **9**

The VLSI design process – Architectural design – Logical design – physical design – Layout styles – Full custom – Semi custom approaches – Basic electrical properties of MOS and CMOS circuits: Ids versus Vds relationships – Transconductance – pass transistor – nMOS inverter – Determination of pull up to pull down ratio for an nMOS inverter – CMOS inverter – MOS transistor circuit model.

UNIT II VLSI FABRICATION TECHNOLOGY **9**

Overview of wafer fabrication – wafer processing – oxidation – patterning – Diffusion – Ion implantation – Deposition – Silicon gate nMOS process – nwell CMOS process – pwell CMOS process – Twintub process – Silicon on insulator.

UNIT III MOS AND CMOS CIRCUIT DESIGN PROCESS **9**

MOS layers – Stick diagrams – nMOs design style – CMOS design style – Design rules and layout – Lambda based design rules – Contact cuts – Double metal MOS process rules – CMOS lambda based design rules – Sheet resistance – Inverter delay – Driving large capacitive loads – Wiring capacitance.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN **9**

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High–speed adders, Multipliers – Physical design – Delay modelling , cross talk, floor planning, power distribution – Clock distribution – Basics of CMOS testing.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE **9**

Overview of digital design with Verilog HDL – hierarchical modeling concepts – modules and port definitions – gate level modeling – data flow modeling – behavioral modeling – task & functions – Test Bench.

L: 45, T: 0, Total: 45

REFERENCES:

1. Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley and Sons, Inc., 2002.
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill Int. Ed., 1990.
5. Bhasker. J., B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
7. Wayne Wolf, "Modern VLSI Design System on chip", Pearson Education,2002.

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140AE0105 **INDUSTRIAL ELECTRONICS** **3 0 0 3**

AIM:

To expose the students to the concepts of various power semiconductor devices and its role in power converter circuits.

OBJECTIVES:

- To impart knowledge on constructional details, principle of operation, characteristics and firing circuit of thyristors, Power MOSFET and IGBT.
- To provide knowledge on principle of operation of power converters used in wind and solar systems.
- To impart knowledge on principle of operation of resonant converters.
- To give exposure on practical applications of converters.

UNIT I POWER SEMICONDUCTOR DEVICES **9**

THYRISTORS: Physics of device operation – Electrical rating – Types of thyristors: Asymmetrical thyristor, Reverse conducting thyristors, light fired thyristors – Turn-on and off mechanisms – Series and parallel operation of thyristors.

POWER MOSFETS: Types – Comparison with BJT – Structure – Principle of operation – Switching characteristics.

IGBTS: Comparison with power BJT and MOSFET – Structure – Principle of working – Switching characteristics – HV IGBT structure – Principle of working – Comparison with GTO.

UNIT II FIRING AND PROTECTION CIRCUITS **9**

Necessity of isolation, pulse transformer, opto coupler – Gate drive circuit: SCR, MOSFET, IGBTs and base drive circuit for power BJT, digital firing schemes – Over voltage, over current and gate protections – Design of snubber circuit.

UNIT III POWER CONVERTERS IN WIND AND SOLAR SYSTEMS **9**

Solar: Block diagram of solar photo voltaic system – Principle of operation: line commutated converters (inversion–mode) – Boost and buck–boost converters – selection of inverter, battery sizing, array sizing.

Wind: Principle of operation: Three phase AC voltage controllers, Uncontrolled and Controlled rectifiers, PWM Inverters, Grid Interactive Inverters, Matrix converters.

UNIT IV RESONANT CONVERTERS **9**

Zero voltage and Zero current switching – Classification of resonant converters –Basic resonant circuit concepts – Load resonant converters – Resonant switch converters – Zero voltage switching, clamped voltage topologies – Resonant DC link Inverters and Zero voltage switching – High frequency link integral half cycle converters.

UNIT V APPLICATIONS **9**

Linear regulators: Switching regulators – Concept of switched mode power supply – Uninterruptible power supply: Different configurations and applications– Speed control of ac and dc drives – Static Circuit Breakers – Solid state relays.

L: 45, T: 0, Total: 45

REFERENCES:

1. Muhammad H. Rashid, "Power Electronics – Circuits, Device and Applications", Pearson, Prentice – Hall of India Private Ltd., New Delhi, 3rd Edition, 2011.
2. Ned Mohan et.al. "Power Electronics – Converters, Applications and Design", John Wiley and Sons (Asia) Private Ltd., 2006.
3. Dubey, G.K., Doradia, S.R., Joshi, A. and Sinha, R.M., "Thyristorised Power Controllers", New age international publishers, 2003.
4. Joseph Vithayathil, "Power Electronics – Principles and Applications", Tata McGraw Hill, 2010.
5. Dr. Bimbhra. P.S., "Power Electronics ", Khanna Publishers, 4th edition, 2008.
6. Mukund R Patel, "Wind and Solar Power Systems", CRC Press, 2004.

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BoS Chairman

140AE0107 APPLIED ELECTRONICS DESIGN LABORATORY I 0 0 3 2

AIM:

To give the experience and practice in using SPICE, MATLAB and HDL to the students.

OBJECTIVES:

- To provide hands-on experience on design and simulation of electronic circuits using PSPICE and MATLAB.
- To provide hands-on experience in FPGA implementations of 4-bit ALU and Real Time Clock.

LIST OF EXPERIMENTS:

1. Design of NMOS/PMOS Logic gates using SPICE.
2. Design of Dynamic latches using SPICE.
3. Design and Simulation of Operational Amplifier using SPICE.
4. Design and Simulation of Analog Multiplier using SPICE.
5. Design of Switched Capacitor filters using SPICE.
6. Design and Simulation of Digital circuits using HDL.
7. FPGA Implementation of 4 Bit ALU.
8. FPGA Implementation of Real Time Clock.
9. Simulation of adaptive and non adaptive digital control system using MATLAB.
10. Design of PLL using MATLAB.

Total: 45

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SEMESTER II

140AE0201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 1 0 4

AIM:

To enhance the knowledge to the students about Bipolar and MOS transistors and their design and analysis for circuit configuration.

OBJECTIVES:

- To understand the models for integrated circuit active devices.
- To study the circuit configuration for linear IC.
- To understand the concepts of operational amplifiers.
- To give an exposure analog multiplier and PLL.
- To develop the knowledge of analog design using MOS technology.

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 12+3

Depletion region of a PN junction – large signal behavior of bipolar transistors – small signal model of bipolar transistor– large signal behavior of MOSFET – small signal model of the MOS transistors – short channel effects in MOS transistors – weak inversion in MOS transistors – substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9+3

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references – Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 8+3

Analysis of operational amplifiers circuit – slew rate model and high frequency analysis – Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL 10+3

Analysis of four quadrant and variable transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise– Noise models of Integrated – circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 6+3

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic – Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

L: 45, T: 15, Total 60

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", 4th Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000.
3. Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuitd", 3rd Edition, McGraw Hill, 2001.
4. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modeling and Technology", Prentice Hall of India pvt. ltd, 2004.
5. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley and sons,Inc.,2003.
6. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition–Oxford University Press, 2003.

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BoS Chairman

140AE0202 **EMBEDDED SYSTEMS** **3 0 0 3**

AIM:

To make students to understand the blocks of embedded system and programming.

OBJECTIVES:

- To deal with product design and characteristics of embedded computer application.
- To know about different controllers and parallel protocols.
- To understand the concept of programming in embedded systems, Routines, Queues, Pointers, etc.,
- To have knowledge about design cycle and tools for development of embedded system.
- To study about real time applications of embedded systems.

UNIT I INTRODUCTION **6**

Building Blocks of an embedded system – Overview of dedicated and automated system and their requirements Characteristics of embedded computer applications – The product design cycle – Design challenges in embedded system Design – Design Technology.

UNIT II PERIPHERALS, MEOMORY AND I/O INTERFACING **12**

Timers, Counter and Watch dog Timer – UART – Pulse Width Modulator – LCD Controllers – Key Pad Controllers – Stepper Motor Controllers – Analog to Digital Converters, Memory Types – ROM –EPROM – EEPROM – Flash Memory – RAM – SRAM – Cache Memory – Memory Management Unit – Interrupts – DMA – Serial Protocols – I^2C – CAN – USB – Parallel Protocols – PCI Bus – ARM Bus.

UNIT III EMBEDDED PROGRAMMING **9**

Programming in Assembly Language (ALP) Vs High level language – C program elements, Macros and Functions – Use of pointers – NULL pointers – use of function calls – multiple function calls in a cyclic order in the main function pointers – Function queues and interrupt service Routines queues pointers – Concepts of Embedded programming in C++ – Object oriented programming – Embedded programming in C++, C program compilers – Cross compiler – optimization of memory codes.

UNIT IV EMBEDDED SYSTEM CO–DESIGN **9**

Embedded System project management – Embedded system design and Co–Design Issues in System Development process – Design cycle in the development phase for an embedded system – Uses of Target system or its emulator and In–Circuit Emulator – Use of software Tools for Development of an embedded system – Use of scopes and logic analyzers for system hardware tests – Issues in Embedded System Design.

UNIT V REAL–TIME OPERATING SYSTEMS **9**

Operating system services – I/O subsystems – Network operating systems – Interrupt Routines in RTOS Environment – RTOS Task scheduling models, Interrupt – Performance Metric in Scheduling Models – IEEE standard POSIX functions for standardization of RTOS and inter – task communication functions – List of Basic functions in a Preemptive scheduler – Fifteen point strategy for synchronization between processors, ISRs, OS Functions and Tasks – OS security issues – Mobile OS.

L: 45, T: 0, Total 45

REFERENCES:

1. Frank Vahid and Tony Givargis, "Embedded System Design: A unified Hardware/ Software Introduction", John Wiley and sons, 2002.
2. Arnold Berger, "Embedded System Design: An Introduction to Processes, Tools & Techniques", CMP Books, Dec 2001.
3. Steve Heath, "Embedded Systems Design", Butterworth – Heinemann, Nov 1997.
4. Wayne Wolf, "Computers as Components: Principles of Embedded Computer Systems Design", Morgan– Kaufmann, Sep 2000.
5. Valvino J W, "Embedded micro computer system: Real time Interfacing", Brooks/ cole, 2000.
6. RajKamal, "Embedded System–Architecture, Programming, Design", Tata McGraw Hill, New Delhi, 2003.

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BoS Chairman

140AE0203 **CAD OF VLSI CIRCUITS** **3 0 0 3**

AIM:

To provide a broad exposure to the algorithms and data structures to generate the layout of modern VLSI design tools.

OBJECTIVES:

- To understand algorithmic graph theory.
- To solve combinatorial optimization problems by various algorithms.
- To know the Algorithms for Placement and Partitioning.
- To study the concepts of floor planning.
- To model and simulate VLSI circuits.
- To know principles of Binary–decision Diagrams.

UNIT I DESIGN METHODOLOGIES **9**

Introduction to VLSI Design methodologies – Review of VLSI Design automation tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – general purpose methods for combinatorial optimization.

UNIT II LAYOUT DESIGN – I **8**

Layout Compaction – Design rules – problem formulation – algorithms for constraint graph compaction – placement and partitioning – Circuit representation – Placement algorithms – partitioning.

UNIT III LAYOUT DESIGN – II **9**

Floor planning concepts – shape functions and floor plan sizing – Types of local routing problems – Area routing – channel routing – global routing – algorithms for global routing.

UNIT IV SIMULATION AND SYNTHESIS **10**

Simulation – Gate–level modeling and simulation – Switch–level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS **9**

High level Synthesis – Hardware models – Internal representation – Allocation – assignment and scheduling – Simple scheduling algorithm – Assignment problem – High level transformations.

L: 45, T: 0, Total 45

REFERENCES:

1. Gerez. S.H., "Algorithms for VLSI Design Automation", John Wiley and Sons,2002.
2. Sherwani. N.A., "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
3. Drechsler, R., "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, Boston, 1998.
4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, Boston, 1989.

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BoS Chairman

140AE0204 **DIGITAL CONTROL ENGINEERING** **3 0 0 3**

AIM:

To enhance knowledge in the advanced concepts of control theory and digital design of control engineering.

OBJECTIVES:

- To understand the basic time and frequency response analysis and discrete time signals.
- To provide adequate knowledge on models of digital control devices and systems.
- To give basic knowledge in obtaining the state variables.
- To understand the concept of stability of control system and methods of stability analysis.
- To study the design of digital control systems.

UNIT I INTRODUCTION **10**

Overview of frequency and time response analysis and specifications of control systems – Digital control systems – basic concepts of sampled data control systems – principle of sampling, quantization and coding – Reconstruction of signals – Sample and Hold circuits – Practical aspects of choice of sampling rate – Basic discrete time signals – Time domain models for discrete time systems.

UNIT II MODELS OF DIGITAL CONTROL DEVICES AND SYSTEMS **9**

Z domain description of sampled continuous time plants – models of A/D and D/A converters – Z Domain description of systems with dead time – Implementation of digital controllers – Digital PID controllers – Position, velocity algorithms – Tuning – Zeigler – Nichols tuning method.

UNIT III STATE VARIABLE ANALYSIS **9**

State space representation of discrete time systems – Solution of discrete time state space equation – State transition matrix – Decomposition techniques – Controllability and Observability – Multi variable discrete systems.

UNIT IV STABILITY ANALYSIS **8**

Mapping between S plane and Z plane– Jury's stability test – Bilinear transformation and extended Routh array– Root Locus Method –Liapunov Stability Analysis of discrete time systems.

UNIT V DESIGN OF DIGITAL CONTROL SYSTEM **9**

Z plane specifications of control system design – Digital compensator design – Frequency response method – State feed back – Pole placement design – State Observers – Digital filter properties – Frequency response – Kalman's filter.

L:45, T: 0, Total 45

REFERENCES:

1. Gopal M. "Digital Control and State Variable methods", Tata Mc Graw Hill Publishing Company Ltd., New Delhi, India, 2003.
2. Kuo B.C. " Digital Control Systems", Oxford University Press, Inc., 2003
3. Ogata K. "Discrete Time Control Systems", Prentice Hall International, New Gercy, USA, 2002.
4. Houpis C.H. and Lamont C.B., "Digital Control Systems", Tata Mc Graw Hill,1999.

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BoS Chairman

140AE0207 **APPLIED ELECTRONICS DESIGN LABORATORY II** **0 0 3 2**

AIM:

To enhance the students knowledge in Microcontrollers and DSP Processors and their applications.

OBJECTIVES:

- To provide hands-on experience in developing the programs using embedded controllers and DSP processors.
- To understand the concepts of interfacing using embedded processors.

LIST OF EXPERIMENTS:

1. LED and Key Matrix interface using Embedded Microcontroller.
2. LCD Interface using Embedded Microcontroller.
3. Rolling Display in LCD /LED using Embedded Microcontroller.
4. EEPROM Interface using Embedded Microcontroller.
5. RTC using Embedded Microcontroller.
6. ADC and DAC Interface using Embedded Microcontroller.
7. Stepper Motor Interface using Embedded Microcontroller.
8. Matrix Multiplication using DSP Processor.
9. Design and Implementation of Convolution Algorithm using DSP Processor.
10. Echo Cancellation using DSP Processor.

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ELECTIVES

140AE9111 PROJECT MANAGEMENT 3 0 0 3

AIM:

To give the exposure to the students on project management, importance of project management and project management tools.

OBJECTIVES:

- To study the basic concepts of project management.
- To acquire knowledge on various project management tools.
- To understand the concepts of project estimation and control.
- To learn application of information systems to project management.

UNIT I PROJECT MANAGEMENT & SYSTEMS AND PROCEDURES 9

Need – Goals– Evolution–different forms–project management in manufacturing, service and government sectors; Systems development cycle – project life cycle – conception phase: proposal , contracting – definition phase – execution phase: production / build, implementation – operation phase– case study. Tools for project planning – work break down structure, responsibility matrix, events and mile stones, Gantt charts.

UNIT II NETWORK SCHEDULING & PERT NETWORK 9

Network Diagram – critical path – late times – slack – float – calendar scheduling. Time estimates – probability of finishing by target completion date – meeting the target – simulating PERT network – – criticisms of PERT ; CPM – Time cost relationship – reducing project duration – shortest duration – total project cost – scheduling with resource constraints – resource loading and leveling – constrained resources: Introduction to GERT network, class studies in PERT/CPM.

UNIT III PROJECT COST ESTIMATION 9

Process – classification–expert opinion, analogy, parametric estimate, cost engineering– example: Contingency amount ; Elements of budgets and Estimates – direct labour, direct non– labour, overhead, general and administrative expenses, profit and total billing; Project cost accounting and management information system – cost summaries, cost schedules and forecasts – case study.

UNIT IV PROJECT CONTROL 9

Cost accounting systems– project control process; Project control emphasis – scope change control, quality control, schedule control, time buffers; Performance Analysis – cost, schedule, work package analysis, performance indices, updating time estimates, technical performance measurement; Performance Index monitoring – variance limits, controlling changes, contract administration, control problems, case study.

UNIT V PROJECT MANAGEMENT INFORMATION SYSTEMS (PMIS) & PROJECT EVALUATION 9

Functions – Computer based PMI Systems – Web–Based project management. Review meetings, reporting, terminating, termination responsibilities, closing the contract, project extensions, project summary evaluation.

L: 45, T: 0, Total 45

REFERENCES :

1. John M Nicholas, "Project Management for Business and Technology", Prentice Hall India Pvt Ltd., New Delhi, 2002.
2. Anastasia Pagnoni, "Project Engineering – Computer Oriented Planning and Operational Decision Making" Springer Verlag, 1990.
3. Parameshwar P Iyer, "Engineering Project Management – with case Studies", Wheeler Publishing, 1996.
4. Dennis Lock, "The Essentials of Project Management", Gower Publishing Ltd., 1996.
5. Vasant Desai, "Project Management", Himalaya Publishing House, 2001.
6. Joseph Phillips, "IT Project Management – On Track from Start to Finish", TMH, 2002.

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BoS Chairman

140AE9112 **ADVANCED MICROPROCESSORS** **3 0 0 3**

AIM:

To enhance the knowledge of advanced processing systems and their features.

OBJECTIVES:

- To understand the architecture of processors.
- To study about Pentium processors and data processing.
- To enhance the knowledge of ARM processors and its operating modes with different interfaces.

UNIT I MICROPROCESSOR ARCHITECTURE **9**

Instruction Set – Data formats –Addressing modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – pipelining – the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM **9**

Introduction to Pentium microprocessor: Real and Protected mode operation – Software model of Pentium – Functional Description – Registers – Data Organization – Summary of 80286, 80386 and 80486 – CPU Architecture – Bus Operations – Pipelining – Branch predication.

UNIT III PENTIUM PROCESSOR PROGRAMMING **9**

Addressing modes – Instruction types – Instruction set – floating point unit – Operating Modes – Paging – Multitasking – Exception and Interrupts – Simple math Programmes.

UNIT IV HIGH PERFORMANCE RISC ARCHITECTURE – ARM **9**

ARM Programmer's Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Introduction to ARM Memory Management Unit.

UNIT V ARM PROCESSOR PROGRAMMING AND BUS STANDARDS **9**

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set overview – Simple assembly language programs. ISA bus, PCI bus, USB – RS232C – IEEE–488 bus.

L: 45, T: 0, Total 45

REFERENCES:

1. Daniel Tabak, "Advanced Microprocessors" McGraw Hill.Inc., 2008.
2. James L. Antonakos , " The Pentium Microprocessor " Pearson Education , 3rd impression,2009.
3. Andrew Sloss , "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2005.
4. Steve Furber, "ARM System–on–Chip Architecture", Pearson Education, 2005.
5. "LPC210x ARM Processor Datasheet" Rev. 5, Philips Electronics, 2004.
6. Badri Ram, "Advanced Microprocessors and Interfacing", Tata McGraw Hill Publishing Company limited, 2007.

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BoS Chairman

140AE9113 **PROGRAMMING WITH VHDL** **3 0 0 3**

AIM:

To enhance the knowledge to the students about the VHDL language for designing the digital integrated circuits.

OBJECTIVES:

- To introduce the fundamentals of VHDL.
- To learn about data types and basic modeling constructs.
- To study the concepts of subprograms, packages and files.
- To study about the signals, components and configurations in VHDL program.
- To implement the VHDL program for designing of programmable logic devices.

UNIT I VHDL FUNDAMENTALS **9**

Fundamental concepts – Modeling digital system – Domain and levels of modeling – modeling languages – VHDL modeling concepts – Scalar Data types and operations– constants and Variable –Scalar Types – Type Classification – Attributes and scalar types – expression and operators–Sequential statements.

UNIT II DATA TYPES AND BASIC MODELING CONSTRUCTS **9**

Arrays – unconstrained array types – array operations and referencing – records – Access Types – Abstract Date types – basic modeling constructs – entity declarations – Architecture bodies – behavioral description – structural descriptions – design Processing, case study: A pipelined Multiplier accumulator.

UNIT III SUBPROGRAMS, PACKAGES AND FILES **9**

Procedures – Procedure parameters – Concurrent procedure call statements – Functions –Overloading – visibility of Declarations – packages and use clauses – Package declarations – package bodies – use clauses – Predefined aliases – Aliases for Data objects – Aliases for Non–Data items – Files – I/O–Files. Case study: A bit vector arithmetic Package.

UNIT IV SIGNALS, COMPONENTS, CONFIGURATIONS **9**

Basic Resolved Signals – IEEE std_Logic_1164 resolved subtypes – resolved Signal Parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – components and configurations – Generate Statements – Generating Iterative structure – Conditionally generating structure – Configuration of generate statements – case study: DLX computer Systems.

UNIT V DESIGN WITH PROGRAMMABLE LOGIC DEVICES **9**

Realization of –Micro controller CPU – Memories– I/O devices–MAC–design, synthesis, simulation and testing.

L: 45, T: 0, Total 45

REFERENCES:

1. Peter J. Ashenden, "The Designer's guide to VHDL", Morgan Kaufmann publishers, San Francisco, 2nd Edition, May 2001.
2. Zainalabedin navabi, "VHDL Analysis ans modeling of Digital Systems", McGraw Hill international Editions, 2nd Edition, 1998.
3. Charles H Roth, Jr. "Digital system Design using VHDL", Thomson, 2006.
4. Douglas Perry, "VHDL Programming by Example", Tata McGraw Hill, 4th Edition 2002.
5. Navabi.Z., "VHDL Analysis and Modeling of Digital Systems", McGraw International, 1998.
6. Peter J Ashendem, "The Designers Guide to VHDL", Harcourt India Pvt Ltd, 2002.
7. Skahill. K, "VHDL for Programmable Logic", Pearson education, 1996.

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BoS Chairman

140AE9114 **DIGITAL IMAGE PROCESSING** **3 0 0 3**

AIM:

To introduce the student to various image processing techniques.

OBJECTIVES:

- To study the image fundamentals for image processing.
- To study the mathematical transforms necessary for the image.
- To study image enhancement and image restoration procedures.
- To study the image segmentation and recognition techniques.
- To study the image compression procedures.

UNIT I DIGITAL IMAGE FUNDAMENTALS **9**

Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS **9**

1D DFT, 2D transforms – DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION **9**

Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic and Yp mean filters – Design of 2D FIR filters. Image restoration – degradation model, Unconstrained and Constrained restoration, Inverse filtering – removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations – spatial transformations, Gray Level interpolation.

UNIT IV IMAGE SEGMENTATION AND RECOGNITION **9**

Image segmentation – Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition – Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Neural networks – Backpropagation network and training, Neural network to recognize shapes.

UNIT V IMAGE COMPRESSION **9**

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.

L:45, T: 0, Total 45

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education, Inc., 2nd Edition, 2004.
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins, " Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
4. Dudgeon. D.E. and Mersereau.R.M., "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.
5. Jayaraman.S., Esakkirajan.S. and Veerakumar.T., "Digital Image Processing", Tata McGraw Hill Ltd., New Delhi, 2010.

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BoS Chairman

140AE9115 **SOFT COMPUTING TECHNIQUES** **3 0 0 3**

AIM:

To provide exposure to the students on various soft computing techniques and their applications in engineering

OBJECTIVES:

- To understand the neural networking concepts and different types of learning.
- To learn the concepts of fuzzy logic system.
- To understand the concepts of genetic algorithm.
- To learn the concepts of optimization techniques and MATLAB toolboxes.
- To build the applications using soft computing techniques.

UNIT I NEURAL NETWORKS **9**

Introduction –Supervised Learning Neural Networks – Perceptrons – Adaline – Back propagation Multilayer perceptrons – Radial Basis Function Networks – Unsupervised Learning and Other Neural Networks – Competitive Learning Networks – Kohonen Self – Organizing Networks – Learning Vector Quantization – Hebbian Learning.

UNIT II FUZZY LOGIC **9**

Introduction to Fuzzy Logic – Fuzzy Sets – Basic Definition and Terminology – Set–theoretic operations – Member Function Formulation and parameterization – Fuzzy Rules and Fuzzy Reasoning – Extension principle and Fuzzy Relations – Fuzzy If–Then Rules – Fuzzy Reasoning – Fuzzy Inference Systems – Mamdani Fuzzy Models – Sugeno Fuzzy Models – Tsukamoto Fuzzy Models – Input Space Partitioning and Fuzzy Modeling.

UNIT III GENETIC ALGORITHM **9**

Genetic algorithm: Basic concept , encoding , fitness function , Reproduction , Basic genetic programming concepts, differences between GA and Traditional optimization methods, Variants of GA, Introduction to Differential Evolution.

UNIT IV EVOLUTIONARY COMPUTATION **9**

Bio Inspired optimization Techniques: Particle Swarm optimization, Ant colony optimization, Bacteria foraging method.

MATLAB Environment for soft computing: Neural Network toolbox, Fuzzy logic toolbox, GA toolbox.

UNIT V APPLICATIONS **9**

Neural Network based multispectral images with SAR Image for Flood Area Analysis – Job Scheduling Problem using GA – Hybrid GA – Fuzzy system for control of Flexible robots – Optimization of Travelling Salesperson Problem using PSO – GA based internet search technique.

L: 45, T: 0, Total 45

REFERENCES:

1. Jang. J.S.R., Sun. C.T. and Mizutan.E.i, "Neuro–Fuzzy and Soft Computing", PHI, Pearson Education 2004.
2. Davis E.Goldberg, "Genetic Algorithms: Search, Optimization and Machine Learning" Addison Wesley, N.Y.,1989.
3. Rajasekaran.S. and Pai.G.A.V. ,"Neural Networks, Fuzzy Logic and Genetic Algorithms", PHI, 2003.
4. Eberhart.R., simpson.P. and Dobbins.R.," Computational Intelligence" PC Tools", AP Professional, Boston 1996.
5. Sivanandam.S.N., Deepa S.N., " Principles of Soft Computing", Wiley–India, 2nd Edition, 2011.

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BoS Chairman

140AE9116 **POWER QUALITY ENGINEERING** **3 0 0 3**

AIM:

To expose the students to the concepts of various power quality problems and its analysis, measurement, monitoring and mitigation techniques.

OBJECTIVES:

- To impart knowledge on categories and characteristics of power system electromagnetic phenomena and various PQ terms.
- To know sources and effects of harmonics and its measurement and mitigation techniques.
- To learn different PQ monitoring techniques and PQ survey.
- To analyze signal processing applications to PQ and custom power devices for PQ enhancement.

UNIT I OVERVIEW OF POWER QUALITY **8**

Definitions: Power quality, Voltage quality – Power quality issues: Short duration voltage variations, Long duration voltage variations, Transients, Waveform distortion, Voltage imbalance, Voltage fluctuation and Power frequency variations – Sources and Effects of power quality problems – Power quality terms – Cost of poor power quality – CBEMA and ITI Curves.

UNIT II WAVEFORM DISTORTION **9**

Introduction – Harmonics indices, Harmonic phase sequences – Sources and effects of harmonic distortion – Harmonics measurement procedure – System response characteristics – Locating Harmonic sources – Principles of controlling harmonics – Devices for controlling harmonic distortion – IEEE and IEC standards.

UNIT III POWER QUALITY MONITORING **9**

Introduction – Need for power quality monitoring, Evolution of power quality monitoring, Deregulation effect on power quality monitoring, Power quality monitoring and the Internet – Applications of intelligent systems: Basic design of an expert system for monitoring applications, Applications of expert systems: Radial fault locator module, Lightning correlation module – Power quality measurement equipments – Planning, Conducting and Analyzing power quality survey, Power Quality Monitoring Standards.

UNIT IV SIGNAL PROCESSING OF PQ DISTURBANCES **10**

Signal processing and power quality – Tools for Harmonic Assessment: Laplace's, Fourier and Hartley transform – The Walsh Transform – Wavelet Transform – Processing of stationary signals: Frequency Domain Analysis and Signal Transformation, Estimation of Harmonics and Interharmonics – Processing of non–stationary signals: Overview of Non–stationary Power Quality Data Analysis Methods, Discrete STFT for Analyzing Time – Evolving Signal Components, Discrete Wavelet Transforms for Time – Scale Analysis of Disturbances.

UNIT V POWER QUALITY IMPROVEMENT **9**

Utility – Customer interface – Harmonic filters: Passive, Active and hybrid filters – Custom power devices: DSTATCOM, DVR and UPQC – Control strategies: PQ theory, Synchronous detection method – Custom power park – Status of application of custom power devices.

L: 45, T: 0, Total 45

REFERENCES:

1. Roger C. Dugan, Mark F. McGranaghan and H.WayneBeaty, "Electrical Power Systems Quality", McGraw–Hill book Co, NewYork, 2nd Edition, 2002
2. Barry W.Kennedy, "Power Quality Primer", McGraw–Hill book Co, New York, 2000.
3. Math H.J.Bollen, Irene Y.H.Gu, "Signal Processing Of Power Quality Disturbances", IEEE Press and John Wiley and Sons, 2006.
4. SurajitChattopadhyay, MadhuchhandaMitra and SamarjitSengupta, "Electric Power Quality" Springer, 2011.
5. AravindamGhosh, Gerard Ledwich, "Power Quality enhancement using custom power devices", Kluwer Academic Publishers, 2002.
6. HirufomiAkagi, Edson HirokazuWatnabe, MauricioAredes, "Instantaneous Power Theory and Applications to Power Conditioning", IEEE Press and John Wiley and Sons, 2007.

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BoS Chairman

140AE9117 **ASIC DESIGN** **3 0 0 3**

AIM:

To know about ASIC design and programming concepts.

OBJECTIVES:

- To understand about CMOS design reules and library architecture.
- To study about programming ASICs clock & power inputs, Xilinx I/o blocks
- Dealing about Altera Max 5000 and 7000, PLA tools and CFI design representation.
- To understand about programming in verilog & VHDL and their simulation.
- Implementation of ASIC design steps physically.

UNIT I INTRODUCTION TO ASICs **9**

Types of ASICs – Design flow – CMOS transistors CMOS Design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

UNIT II PROGRAMMABLE ASICs **9**

Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks.

UNIT III INTERCONNECTS AND DESIGN TOOLS **9**

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX – Design systems – Logic Synthesis – Half gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF– CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Verilog and logic synthesis – VHDL and logic synthesis – types of simulation – boundary scan test – fault simulation – automatic test pattern generation.

UNIT V PHYSICAL DESIGN **9**

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC.

L: 45, T: 0, Total 45

REFERENCES:

1. Smith. M.J.S., "Application Specific Integrated Circuits", Addison –Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. Wayne Wolf, "FPGA–Based System Design", Prentice Hall PTR, 2004.
4. Baskar.J , "VHDL Primer", McGraw Hill, 2005
5. Doughles L.Perry, "VHDL Programming by Example", McGraw Hill Professional, 4th Edition, 2002.

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BoS Chairman

140AE9118 DATA COMMUNICATION NETWORKS 3 0 0 3

AIM:

To give the exposure to the students on computer networking, different layers and their associated protocols, and internetworking concepts.

OBJECTIVES:

- To learn the basic concepts and basic layering of computer networks.
- To know the protocols of the associated layers and their use.
- To understand the concepts of internetworking and relevant protocols.

UNIT I INTRODUCTION **4**

Definition of Networks – Classification of Networks – LAN, MAN, WAN, internet – Network Topology – Protocols and Standards – Network Models – OSI, TCP/IP Models of networking – Internet.

UNIT II PHYSICAL LAYER AND THE MEDIA **10**

Review of Signals – Data Rate Limits – Performance Issues – Bandwidth, Throughput, Latency, Bandwidth – Delay Product, Jitter. Digital Transmission and Analog Transmission: Line coding techniques, PCM and Delta Modulation techniques – ASK, FSK, PSK, and QAM Techniques – Bandwidth Utilization: Multiplexing and Spreading – Data Transmission using Telephone Networks – Dial–up MODEMS, Digital Subscriber Line (DSL).

UNIT III DATA LINK LAYER **10**

Error Detection and Correction techniques – Data Link Control: Framing, Flow and Error Control – HDLC and PPP protocols. Multiple Access Techniques – CSMA, CSMA/CD, CSMA/CA – Channelization – TDMA, FDMA, and CDMA.

UNIT IV LANS AND WANS **12**

Wired LANs – IEEE 802 standards – Ethernet – IEEE 802.3 MAC Frame – Token Ring LAN – IEEE 802.5 MAC Frame – Wireless LANs – IEEE 802.11 standard – Bluetooth Technology – Interconnection of LANs.

Wired WANs – Circuit-Switched Networks, Datagram Networks, Virtual Circuit-Switched Networks, Structure of Circuit and Packet Switches – Wireless WANs – Introduction to Cellular Telephone and Satellite networks.

UNIT V INTERNETWORKING **9**

Internetworking – tunneling – IP Addressing Scheme – Structure of IP Datagram – IP Routing – TCP as Transport Layer Protocol – Structure of TCP Segment – TCP Connection: Establishment and Closing – SMTP Protocol for E–Mail Application.

L: 45, T: 0, Total 45

REFERENCES:

1. Behrouz A. Forouzan, " Data Communications and Networking", 4th Edition, Tata McGraw–Hill, New Delhi, 2006
2. Larry L. Peterson and Bruce S. Davie, "Computer Networks: A Systems Approach", 4th Edition, Elsevier Publications, New Delhi, 2007
3. Stanford H. Rowe and Marsha L. Schuh, "Computer Networking", Pearson Education, New Delhi, 2005.
4. James Kurose and Keith Ross," Computer Networking : Top Down Approach featuring the Internet", Pearson Education, New Delhi,2002.

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BoS Chairman

140AE9119 VIRTUAL INSTRUMENTATION SYSTEMS 3 0 0 3

AIM:

To understand Virtual Instrument systems concepts and study computer interface system.

OBJECTIVES:

- To understand the concept of virtual instruments and prerequisites for a computer leased instrument systems.
- To illustrate Lab VIEW environment and graphical programming concepts.
- To explore the different Data acquisition hardware and interfaces, configuration and features.

UNIT I INTRODUCTION **8**

General Functional description of a digital instrument – Block diagram of a Virtual Instrument – Physical quantities and Analog interfaces – Hardware and Software – User interfaces – Advantages of Virtual instruments over conventional instruments – Architecture of a Virtual instrument and its relation to the operating system.

UNIT II SOFTWARE OVERVIEW **10**

Lab VIEW – Graphical user interfaces – Controls and Indicators – 'G' programming – Data types – Data flow programming – Editing – Debugging and Running a Virtual instrument – Graphical programming pallets – Front panel objects – Controls, Indicators, Object properties and their configuration – Typical examples.

UNIT III PROGRAMMING STRUCTURE **8**

FOR loops, WHILE loop, CASE structure, formula node, Sequence structures – Arrays and Clusters – Array operations – Bundle – Bundle/Unbundle by name, graphs and charts – String and file I/O – High level and Low level file I/O's – Attribute modes Local and Global variables.

UNIT IV HARDWARE ASPECTS **9**

Installing hardware, installing drivers – Configuring the hardware – Addressing the hardware in Lab VIEW – Digital and Analog I/O function – Data Acquisition – Buffered I/O – Real time Data Acquisition.

UNIT V LABVIEW APPLICATIONS **10**

Motion Control: General Applications – Feedback devices, Motor Drives – Machine vision – Lab VIEW IMAQ vision – Machine vision Techniques – Configuration of IMAQ DAQ Card – Instrument Connectivity – GPIB, Serial Communication – General, GPIB Hardware & Software specifications – PXI / PCI: Controller and Chassis Configuration and Installation.

L: 45, T: 0, Total 45

REFERENCES:

1. Garry W Johnson, "LabView Graphical Programming", Tata McGraw Hill, 3rd Edition, 2001.
2. Sanjay Gupta and Joseph John, "Virtual Instrumentation Using LabVIEW", Tata McGraw–Hill, Ist Edition, 2008.
3. LabView: Basics I & II Manual, National Instruments, 2006
4. Barry Paron, "Sensors, Transducers and LabVIEW", Prentice Hall , 2000.
5. William Buchanan and Bill Buchanan, "Computer Basics", CRC Press, 2000.

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BoS Chairman

140AE9120 **NANO COMPUTING** **3 0 0 3**

AIM:

To give the exposure to the students on nano electronics, nano computing and their architectures.

OBJECTIVES:

- To learn the basic concepts of nano computing.
- To acquire knowledge on biochemical and quantum–mechanical computers.
- To understand the concepts of parallel architectures and nano electronics.
- To learn about information processing systems.

UNIT I INTRODUCTION **10**

The development of Microelectronics – The region of Nanoelectronics – The Complexity Problem – The challenge initiated by Nanoelectronics – Basics of Nanoelectronics: Electromagnetic Fields and Photons – Quantization of Action, Charge, and Flux – Electrons behaving as waves – Electrons in potential wells – D diffusion Process.

UNIT II BIOCHEMICAL AND QUANTUM–MECHANICAL COMPUTERS **8**

DNA Computer – Information Processing with Chemical reactions – Nanomachines – Parallel Processing – Quantum Computers – Bit and Qubit – Coherence and Entanglement – Quantum Parallelism.

UNIT III PARALLEL ARCHITECTURES FOR NANOSYSTEMS **9**

Mono and Multiprocessor Systems – Some considerations to Parallel Processing – Influence of Delay Time – Power Dissipation – Architecture for Processing in Nanosystems: Clasic Systolic Arrays – Processor with large memory – Processor array with SIMD and PIP Architectures – Reconfigurable Computers – The Teramac Concept as a Prototype.

UNIT IV SOFT COMPUTING AND NANOELECRONICS **9**

Methods of Soft Computing – Fuzzy Systems – Evolutionary Algorithms – Connectionistic Systems – Computationally Intelligent Systems – Characteristics of Neural Networks in Nanoelectronics – Local Processing – Distributed and Fault–tolerant Storage – Self–organization.

UNIT V NANOSYSTEMS AS INFORMATION PROCESSING MACHINES **9**

Nanosystems as Functional Machines – Information Processing as Information Modification – System Design and its interfaces – Requirements of Nanosystems. Uncertainties: Removal of Uncertainties by Nanomachines – Uncertainties in Nanosystems – Uncertainties in the Development of Nanoelectronics.

L: 45, T: 0, Total 45

REFERENCE:

1. Karl Goser et.al, "Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum devices", Springer, New Delhi, 2005.

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BoS Chairman

140AE9121 **VLSI SIGNAL PROCESSING** **3 0 0 3**
(Common to AE and CM Programmes)

AIM:
To enhance knowledge in VLSI design and signal processing.

OBJECTIVES:
- To introduce DSP systems, filters & processing.
- To emphases on retiming, parallel filters.
- To exposure on convolution methods & HR filters.
- To discussion about Bit–level arithmetic architectures, Lyon's bit serial multipliers.
- To get an idea about sub expression elimination, wave pipelining.

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS **9**
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION **9**
Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2–parallel FIR filter, 2–parallel fast FIR filter, DCT architecture, rank–order filters, Odd–Even merge–sort architecture, parallel rank–order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS **9**
Fast convolution – Cook –Toom algorithm, modified Cook – Toom algorithm, Pipelined and parallel recursive filters – Look–Ahead pipelining in first–order IIR filters, Look – Ahead pipelining with power of 2 decomposition, Clustered look – ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV SCALING, ROUND–OFF NOISE, BIT–LEVEL ARITHMETIC ARCHITECTURES **9**
Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit–serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING **9**
Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge – triggered single phase clocking, two – phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

L: 45, T: 0, Total 45

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. Meyer. U – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

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BoS Chairman

140AE9122 HIGH PERFORMANCE SWITCHING ARCHITECTURES 3 0 0 3

AIM:

To enhance the knowledge of the students on computer network switching architecture and performance improvement.

OBJECTIVES:

- To learn LAN switching technologies.
- To understand the different switching architectures.
- To know the concepts of IP switching.

UNIT I LAN SWITCHING TECHNOLOGY **9**

Switching Concepts – switch forwarding techniques – switch path control – LAN Switching, cut through forwarding – store and forward – virtual LANs.

UNIT II ATM SWITCHING ARCHITECTURE **9**

Blocking networks – basic and enhanced banyan networks, sorting networks – merge sorting, re–arrangable networks – full and partial connection networks, non blocking networks – Recursive network construction, comparison of non–blocking network, Switching with deflection routing – shuffle switch, tandem banyan switch.

UNIT III QUEUES IN ATM SWITCHES **9**

Internal Queueing –Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing – performance analysis of Queued switches.

UNIT IV PACKET SWITCHING ARCHITECTURES **9**

Architectures of Internet Switches and Routers – Bufferless and buffered Crossbar switches, Multi–stage switching, Optical Packet switching; Switching fabric on a chip; Internally buffered Crossbars.

UNIT V IP SWITCHING **9**

Addressing model, IP Switching types – flow driven and topology driven solutions, IP over ATM address and next hop resolution, multicasting, IPv6 over ATM.

L: 45, T: 0, Total 45

REFERENCES:

1. Achille Pattavina, "Switching Theory: Architectures and performance in Broadband ATM networks ",John Wiley & Sons Ltd, New York. 1998
2. Elhanany M. Hamdi, "High Performance Packet Switching architectures", Springer Publications, 2007.
3. Christopher Y Metz, "Switching protocols & Architectures", McGraw Hill Professional Publishing, NewYork.1998.
4. Rainer Handel, Manfred N Huber, Stefan Schroder, "ATM Networks – Concepts Protocols, Applications", 3rd Edition, Addison Wesley, New York. 1999.

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BoS Chairman

140AE9123 **MEMS SYSTEM DESIGN CONCEPTS** **3 0 0 3**

AIM:

To gain knowledge about MEMS design and circuit system issues and their operations.

OBJECTIVES:

- To introduce Microsystems and micro actuators.
- To dealing about material properties and configuration.
- To have an adequate knowledge about basic theory in electronics, electromagnetic actuators.
- To learn about circuit design interfaces and modelling of systems.
- To introduce about system design basics and relative case studies.

UNIT I INTRODUCTION TO MEMS **9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN **9**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN **9**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES **9**

Electronic Interfaces, Feedback systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS **9**

Optical MEMS, – System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Mems – design basics, case study – Capacitive RF MEMS switch, performance issues.

L: 45, T: 0, Total 45

REFERENCES:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
3. Mohamed Gad–el–Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

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BoS Chairman

140AE9124 WAVELET TRANSFORMS AND ITS APPLICATIONS 3 0 0 3

AIM:

To gain knowledge about wavelet transform, CWT, DWT and their applications.

OBJECTIVES:

- To introduce vector spaces and their properties.
- To have an adequate knowledge in Fourier analysis.
- To learn continuous wavelet transform, discrete wavelet transform and their applications.

UNIT I INTRODUCTION **9**

Vector spaces – properties – dot product – basis – dimension, orthogonality and orthonormality – relationship between vectors and signals – signal spaces – concept of convergence – Hilbert spaces for energy signals – Generalized Fourier expansion.

UNIT II FOURIER ANALYSIS **9**

Fourier Transform – drawbacks of Fourier analysis–Short–time Fourier Transform (STFT) analysis–spectrogram plot–phase–space plot in time–frequency plane – Time and frequency limitations–uncertainty principle – Tilling of the time–frequency plane for STFT.

UNIT III CONTINUOUS WAVELET TRANSFORM **9**

Wavelet transform – properties – concept of scale and its relation with frequency – Continuous Wavelet Transform (CWT) – scaling function and wavelet functions: Daubechies, Haar, Coiflet, Mexican hat, Sine, Gaussian, Bi–orthogonal – Tilling of time scale plane for CWT.

UNIT IV DISCRETE WAVELET TRANSFORM **9**

Discrete Wavelet Transform (DWT) – Filter bank and sub–band coding principles – Multi-resolution analysis – Time scale difference equations for wavelets and scaling functions – Wavelet filters – scale variation in discrete domain – Mallet's algorithm for DWT – Inverse DWT computation by filter banks –multi-band wavelet transform.

UNIT V CASE STUDIES **9**

Sub–band coding of images – Image compression – Image denoising – Detection of sag, tilt, swells and surge in power signal – Fractal signal analysis

L: 45, T: 0, Total 45

REFERENCES:

1. Strang G Nguyen T., "Wavelets and Filter Banks", Wellesley Cambridge Press, 1996.
2. Vetterli M, Kovacevic J., "Wavelets and Sub–band Coding", Prentice Hall, 1995.
3. Mallat S., "A Tour on Wavelet Signal Processing", Elsevier, New Delhi, December 2005.
4. Rao .R.M and Bopardikar.A.S, "Wavelet Transforms", Addison Wesley, 1999.
5. Soman. K.P. and Ramachandran. K.I. "Insight into Wavelets–From Theory to Practice", Prentice Hall of India, 2005.
6. Meyer Y et.al., "Wavelet Toolbox Manual", Mathworks Inc., 1995.

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BoS Chairman

140AE9125 LOW POWER VLSI DESIGN 3 0 0 3

AIM:

To learn about power dissipation, optimization & estimation in low power VLSI design techniques.

OBJECTIVES:

- To learn source of power consumption and basic principle of low power design.
- To deal about circuit techniques for reducing power consumption.
- To emphasis on layout design, advanced techniques, and special techniques.
- To analysis of power estimation and power analysis techniques.
- To exposure on software design for low power.

UNIT I POWER DISSIPATION IN CMOS **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9**

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION **9**

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power –Behavioral level transforms– Software design for low power.

L: 45, T: 0, Total 45

REFERENCES:

1. Roy. K. and Prasad. S.C. , "LOW POWER CMOS VLSI circuit design", Wiley,2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis," Designing CMOS Circuits For Low Power", Kluwer,2002.
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer,1998.
4. Chandrakasan. A.P., Broadersen. R.W, "Low Power Digital CMOS VLSI Design", Kluwer 1995.

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BoS Chairman

140AE9126 **INTERNETWORKING AND MULTIMEDIA** **3 0 0 3**
(Common to AE and CM Programmes)

AIM:
To give the exposure to the students on the concepts of interworking, multimedia and relevant protocols, and applications.

OBJECTIVES:
- To study the basic concepts of multimedia networking.
- To learn about multicast and transport protocol.
- To understand the concepts of multimedia servers.
- To know the applications of multimedia and interworking.

UNIT I MULTIMEDIA NETWORKING **9**
Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY **9**
Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL **9**
Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA – ON – DEMAND **9**
Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS **9**
MIME, Peer–to–peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

L: 45, T: 0, Total 45

REFERENCES:

1. Jon Crowcroft, Mark Handley, Ian Wakeman. "Internetworking Multimedia", Harcourt Asia Pvt.Ltd. Singapore, 1998.
2. Szuprowicz. B.O., "Multimedia Networking", McGraw Hill, New York. 1995.
3. Tay Vaughan," Multimedia making it to work", 4ed, Tata McGraw Hill, New Delhi, 2000.

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BoS Chairman

140AE9127 **ALGORITHM ANALYSIS AND DESIGN** **3 0 0 3**

AIM:

To give the exposure to the students on algorithm design techniques and basic problem types.

OBJECTIVES:

- To learn the fundamentals of algorithm design concepts.
- To understand the basics of different algorithm design techniques.
- To know the concepts of different sorting and searching techniques and their complexities.
- To study the graph algorithms and advanced concepts in algorithm designing.

UNIT I INTRODUCTION **9**

Introduction – Notion of Algorithm – Fundamentals of algorithmic problem solving – Important problem types – Fundamentals of the analysis of algorithm efficiency – analysis frame work – Asymptotic notations – Mathematical analysis for recursive and non–recursive algorithms.

UNIT II DIVIDE AND CONQUER METHOD AND GREEDY METHOD **9**

Divide and conquer methodology – Merge sort – Quick sort – Binary search – Binary tree traversal – Multiplication of large integers – Strassen's matrix multiplication – Greedy method– Prim's algorithm – Kruskal's algorithm – Dijkstra's algorithm.

UNIT III DYNAMIC PROGRAMMING **9**

Computing a binomial coefficient – Warshall's and Floyd' algorithm – Optimal binary search tree – Knapsack problem – Memory functions.

UNIT IV BACKTRACKING AND BRANCH AND BOUND **9**

Backtracking – N – Queens problem – Hamiltonian circuit problem – Subset sum problem – Branch and bound – Assignment problem – Knapsack problem Traveling salesman problem.

UNIT V NP–HARD AND NP–COMPLETE PROBLEMS **9**

P & NP problems – NP– complete problems – Approximation algorithms for NP– hard problems – Traveling salesman problem – Knapsack problem.

L: 45, T: 0, Total: 45

REFERENCES:

1. Anany Levitin "Introduction to the Design and Analysis of Algorithms", Pearson Education 2003.
2. Thomas H.Cormen, Charles E.Leiserson, Ronald L.Rivest, "Introduction to algorithms" , Prentice Hall 1990.
3. SaraBaase and Allen Van Gelder, "Computer Algorithms – Introduction to Design and Analysis" Pearson education, 2003.
4. Aho. A.V., Hopenfit J.E and Ullman. J.D., "The Design and Analysis of Computer algorithms" Pearson education Asia, 2003.

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BoS Chairman

140AE9128 **RESEARCH METHODOLOGY** **3 0 0 3**

(Common to AE and CM Programmes)

AIM:

To study the context of planning and development, that the significance of research lies in its quality.

OBJECTIVES:

- To enable researchers, in developing the most appropriate methodology for their research studies.
- To make the researchers familiar with the art of using different research methods and techniques.
- To study the different methods of data collection, measurement and scaling techniques.
- To understand the several parametric tests of hypotheses.
- To study the analysis of data and the art of writing research reports.

UNIT I INTRODUCTION AND DATA COLLECTION **9**

Research methodology – definition, mathematical tools for analysis, Types of research, exploratory research, conclusive research, modelling research, algorithmic research, Research process – steps. Data collection methods – Primary data – observation method, personal interview, telephonic interview, mail survey, questionnaire design – Secondary data – internal sources of data, external sources of data.

UNIT II SCALES AND SAMPLING **9**

Scales – measurement, Types of scale – Thurstone's Case V scale model, Osgood's Semantic Differential scale, Likert scale, Q– sort scale. Sampling methods– Probability sampling methods – simple random sampling with replacement, simple random sampling without replacement, stratified sampling, cluster sampling. Non–probability sampling method – convenience sampling, judgment sampling, quota sampling.

UNIT III HYPOTHESES TESTING–I (PARAMETRIC TESTS) **9**

Hypotheses testing – Testing of hypotheses concerning means (one mean and difference between two means – one tailed and two tailed tests), concerning variance – one tailed Chi–square test.

UNIT IV HYPOTHESES TESTING–II (NONPARAMETRIC TESTS) **9**

Nonparametric tests – One sample tests – one sample sign test, Kolmogorov – Smirnov test, run test for randomness, Two sample tests – Two sample sign test, Mann – Whitney U test, K– sample test – Kruskal Wallis test (H – Test).

UNIT V DATA ANALYSIS AND REPORT PREPARATION **9**

Introduction to Disciminant analysis, Factor analysis, cluster analysis, multidimensional scaling, conjoint analysis. Report writing – Types of report, guidelines to review report, typing instructions, oral presentation.

L: 45, T: 0, Total 45

REFERENCES:

1. Kothari, C.R., "Research Methodology –Methods and techniques", New Age Publications, New Delhi, 2009.
2. Panneerselvam, R., "Research Methodology", Prentice–Hall of India, New Delhi, 2004.

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BoS Chairman

140AE9129 SPEECH AND AUDIO SIGNAL PROCESSING 3 0 0 3

AIM:

The aim of this course is to build up a familiarity with the perceptually–salient aspects of the audio signal, and how they can be extracted and manipulated through signal processing.

OBJECTIVES:

- To provide comprehension on the foundations of speech processing.
- To obtain a thorough understanding of the statistical pattern recognition technology at the core of contemporary speech and audio processing systems.
- To deepen student's familiarity with the acoustics and auditory perception.
- To obtain an understanding of the speech & audio recognition systems and speech features.
- To provide basics for the designing of voice coders in different applications.

UNIT I INTRODUCTION **9**

Speech Analysis and Synthesis Overview – Radio rex, digit recognition – Speech recognition overview – Z Transform – Difference Equations – Digital Filters: Filtering concepts, filter functions, transformations for filter design – digital filter design with bilinear transformation.

UNIT II PATTERN CLASSIFICATION **9**

Feature extraction – Pattern Classification Methods: Minimum distance, discriminant functions, generalized discriminators, multilayer perception training – Statistical Pattern Recognition: Class –related probability functions, minimum error classification, likelihood – based MAP classification – approximating a Bayes classifier, linear discriminants, EM algorithm.

UNIT III ACOUSTICS AND AUDITORY PERCEPTION **9**

Wave Basics: Wave equations, traveling and standing waves, acoustic tube models, excitation mechanisms in speech production – Music production – room acoustics – Auditory Perception: Models of pitch perception, speech perception, human speech recognition.

UNIT IV SPEECH FEATURES AND AUTOMATIC SPEECH RECOGNITION **9**

Speech Features: Auditory system as a filter bank, cepstrum as a spectrum analyzer, linear prediction – Automation speech recognition: Feature extraction for ASR, linguistic categories for speech recognition, speech recognition and understanding.

UNIT V SYNTHESIS AND CODING **9**

Parametric source – filter synthesis, concatenative methods – Pitch detection – Vocoders – low, medium and high rate Vocoders

L: 45, T: 0, Total: 45

REFERENCES:

1. Ben Gold and Nelson Morgan, "Speech and Audio Signal Processing" Wiley–India Edition, 2007
2. Rabiner. L.R. and Schaffer. R.W. "Digital Processing of Speech signals", Prentice Hall,1978
3. Quatieri," Discrete–time Speech Signal Processing", Prentice Hall, 2001.
4. Flanagan. L., "Speech analysis: Synthesis and Perception",2nd edition, Berlin, 1972
5. Witten. I.H. , "Principles of Computer Speech", Academic Press,1982
6. Simon Haykin, "An Introduction to Analog and Digital Communications", Wiley–India Edition, 2010.

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BoS Chairman